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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/811,806	03/30/2004	Siva G. Narendra	INTEL-0038	2840

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EXAMINER	
BOATENG, ALEXIS ASIEDUA	
ART UNIT	**PAPER NUMBER**
2838	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/811,806	NARENDRA ET AL.	
	Examiner	Art Unit	
	Alexis Boateng	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 November 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2, 6, 10, 11, 13, 14, 16, 17, 20, 25, 27 - 38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2, 6, 10, 11, 13, 14, 16, 17, 20, 25, 27 - 38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 2, 6, 9, 10, 11, 13, 16, 17, 20, 29 – 34, and 36 – 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe (U.S. 2001/0054881) in view of Bean (U.S. 2004/0036449).

Regarding claims 1, 7, 14, and 25, Watanabe discloses wherein a system comprising:

a detector to detect a voltage stored in an ultracapacitor (paragraph [0065]); and

an extractor to extract energy from the ultracapacitor, the extractor including: a first amplifier circuit to amplify an output voltage from the ultracapacitor when the detected voltage falls below a first predetermined voltage of a load coupled to the ultracapacitor (paragraphs [0069] – [0070]);

a divider to divide the amplified voltage form a first control signal for the first amplifier circuit (paragraph [0092] – [0093]); and

a controller to generated a second control signal to vary a ratio of the divider, the varied ratio adjusting the first control signal to maintain the output voltage of the ultracapacitor substantially equal to or above the first

predetermined voltage of the load, the first amplifier circuit to amplify the output voltage independent of a charging operation of the ultracapacitor and during a time when the load it to be driven by the amplified output voltage (figure 1 item 13, paragraph [0069]). Watanabe discloses the invention as claimed but does not disclose the remainder. Bean discloses in figure 1 item 110, wherein the power supply is an ultracapacitor based power supply. At the time of invention, it would have been obvious to a person of ordinary skill in the art to modify the Watanabe system with the Bean system so the system may operate in a portable manner.

Regarding claim 2, Watanabe discloses wherein a system wherein the first amplifier circuit is to amplify said output voltage of the ultracapacitor to a level substantially equal to or above the first predetermined voltage during a time then the detected voltage of the ultracapacitor is above a second predetermined voltage of the first amplifier circuit (paragraph [0085]).

Regarding claim 6, Watanabe discloses wherein a second amplifier circuit to adjust impedance of the amplified voltage output from the first amplifier circuit (figure 1 item 22).

Regarding claim 9, Watanabe wherein the extractor further comprises a voltage regulator to adjust the changed voltage to maintain the first predetermined voltage (paragraph [0163] – [0164]).

Regarding claim 10, Watanabe discloses wherein a detector to detect a voltage in an ultracapacitor; and

an extractor to extract energy from the ultracapacitor, the extractor including an adiabatic amplifier to amplify voltage output form the ultracapacitor when the detected voltage falls below a first predetermined voltage of a load coupled to the ultracapacitor, wherein the adiabatic amplifier includes (figure 1 items 4A-D; paragraph [0069]):

first and second transmission gates that are alternatively switched output an amplified differential signal that corresponds to the amplifier voltage of the ultracapacitor, wherein the adiabatic amplifier is to amplify the voltage output from the ultracapacitor independent of a charging operation of the ultracapacitor and during a time when the load is to be driven by the amplified output voltage (figure 1 items 4A-D; paragraphs [0076] and [0090] voltage of load capacitor is boosted then it is recharged. Therefore, the boosted voltage is independent of charging the capacitor).

Regarding claim 11, Watanabe discloses wherein a controller to monitor a change in the amplified voltage (figure 1 item 13); and

a voltage regulator to adjust the amplified differential signal to cause the amplified voltage of the ultracapacitor to be substantially equal to or above the first predetermined voltage (paragraph [0163]).

Regarding claim 13, Watanabe discloses wherein the extractor is a DC-DC boost converter (paragraph [0069]).

Regarding claim 16, Watanabe discloses wherein the varied ratio adjusts the first control signal to maintain the output voltage of the ultracapacitor

substantially equal to or above the first predetermined voltage during a time when the detected voltage of the ultracapacitor is above a second predetermined voltage of an amplifier circuit that is to perform said amplifying (paragraphs [0092], [0092] and [0102]).

Regarding claim 17, Watanabe discloses wherein detecting a reduction in the increased voltage over time; and adjusting the reduced voltage to maintain at least the predetermined voltage of the load (figure 20 item 2).

Regarding claim 20, Watanabe discloses wherein said amplifying is performing by a circuit, which includes an adiabatic amplifier (figure 1 items 4A-D).

Regarding claims 29 – 34, Watanabe discloses wherein the first predetermined voltage corresponds to a minimum operating voltage of the load (paragraph [0008] and [0068] – [0069]).

Regarding claims 36 – 38, Watanabe discloses wherein the divider includes a network of variable resistors (paragraphs [0093] and [0102] – [0103]; figure 1 items 9 and 10).

3. Claims 27, 28 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe (U.S. 2001/0054881) in view of Bean (U.S. 2004/0036449) applied to claim 25 and in further view of Sasaki (U.S. 6,476,587).

Regarding claim 27, Watanabe and Bean do not disclose the invention as claimed. Sasaki discloses wherein the load is at least on of a power supply, processor, cache, chipset and a memory (figure 3 shows wherein the system is used to charge the components of a mobile device which includes a power

supply, processor, cache, chipset and memory). At the time of invention, it would have been obvious to a person of ordinary skill in the art to modify the Watanabe and the Bean system with the Sasaki system so that the system maybe used within a variety of applications.

Regarding claim 28, Watanabe and Bean do not disclose the invention as claimed. Sasaki discloses wherein the load, ultracapacitor and extractor are included on a single die (figure 1). At the time of invention, it would have been obvious to a person of ordinary skill in the art to modify the Watanabe and Bean system with the Sasaki system so that the system may be used in mobile applications.

Regarding claim 35, Watanabe and Bean do not disclose the invention as claimed. Sasaki discloses in column 2 lines 63 – column 3 line 24 wherein the load is connected to path when it is above the first predetermined voltage level and disconnected when its below the first predetermined voltage level. At the time of invention, it would have been obvious to a person of ordinary skill in the art to modify the Watanabe and Bean system with the Sasaki system so that proper charging is ensured and the system is not damaged by overdischaging.

Response to Arguments

4. Applicant's arguments filed 11/01/07 have been fully considered but they are not persuasive. **Regarding claim 1,** the applicant argues that the Watanabe system does not disclose or suggest wherein a control circuit varies the ration of its voltage divider in

order to maintain an output voltage equal to or above a voltage of a load. Watanabe discloses in paragraphs [0092] – [0093] and in figure 7 wherein the voltage that is divided (Vd) is multiplied by the voltage boost portion of the charge Vc. This multiplication of the divided voltage varies the voltage within the system. It has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. *Ex parte Masham,* 2 USPQ2d 1647 (1987). **Regarding claim 10,** the applicant argues that the Watanabe reference does not disclose wherein the voltage is amplified. Watanabe discloses in paragraph [0076] wherein the IGBTs boost the charge voltage. The applicant also argues that the Bean reference does not read upon the Watanabe reference. Claim 10 is only rejected upon the Watanabe reference. **Regarding claim 11,** the applicant argues that the Watanabe reference does not monitor a change in voltage. Watanabe discloses in paragraphs [0007] and [0069] wherein the change in voltage detected from the voltage divider, items 9 and 10 and then a signal is sent by the inverter controller. The inverter controller cannot work independently from the voltage divider, so it plays a part in detecting the change in voltage. **Regarding claim 16,** the applicant argues that Watanabe does not disclose adjusting a first control signal to maintain the output voltage of the ultracapacitor substantially equal to or above the first predetermined voltage during a time when the detected voltage of the ultracapacitor is above a second predetermined voltage of an amplifier circuit that is to perform said amplifying. Watanabe discloses in paragraphs [0092] – [0093] and in figure 7 wherein the voltage

that is divided (Vd) is multiplied by the voltage boost portion of the charge Vc. This multiplication of the divided voltage varies the voltage within the system. It has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. *Ex parte Masham,* 2 USPQ2d 1647 (1987). **Regarding claims 27, 28, and 35,** the applicant argues that the Sasaki patent does not teach or suggest the features of claims 1 and 25. Sasaki discloses detecting the voltage of the ultracapacitor, figure 1 item 21. Sasaki further discloses in column 2 line 55 – column 3 line 63 wherein the charge from the ultracapcitor is increased when it gets low and provided to the load.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexis Boateng whose telephone number is (571) 272-5979. The examiner can normally be reached on 8:30 am - 6:00 pm, Monday - Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ullah Akm can be reached on (571) 272-2361. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AB

BAO Q. VU
PRIMARY EXAMINER